

JMT3801N

Product Preview

25V 10A Dual N-Channel MOSFET



Features

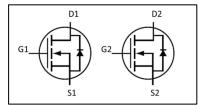
- Advanced shielded-gate technology
- Ultra-low on-resistance and gate-charge
- RoHS compliant
- 100% avalanche tested

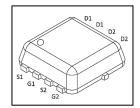


Product Summary				
V _{DS}	25V			
D	9.8mΩ (Typ.)			
R _{DS(ON)}	12mΩ (Max.)			
I _D	10A			

Applications

- Motor controllers
- DC-to-DC convertors
- Battery-driven electronic products, electrical equipment and machines





Ordering Information

Part Number	Marking	Package	Packaging
JMT3801N	MT3801N	DFN3.3x3.3 dual	Tape & Reel



Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Drain-to-Source Voltage	V _{DS}	25	V
Gate-to-Source Voltage	V_{GS}	±10	V
Continuous Drain Current, Package Limited (T _C = 25°C) (1)	I _D	10	
Continuous Drain Current (T _C = 25°C) (1)	I _D	40	
Continuous Drain Current (T _C = 100°C) (1)	I _D	24	_
Continuous Drain Current (T _A = 25°C) (2), (6)	I _D	11	A
Continuous Drain Current (T _A = 100°C) (2), (6)	I _D	6	
Pulsed Drain Current (3)	I _{DM}	160	
Power Dissipation (T _C = 25°C)	P _D	26	W
Linear Derating Factor	-	0.21	W/°C
Single Pulse Avalanche Energy (4)	E _{AS}	17	mJ
Avalanche Current (5)	I _{AS}	13	Α
Junction Temperature	T _J	-55 to 150	°C
Storage Temperature	T _{STG}	-55 to 150	

Thermal Characteristics

Parameter	Symbol	Max	Unit
Junction-to-Ambient Thermal Resistance (6)	$R_{\theta JA}$	62	°C /\\
Junction-to-Case Thermal Resistance	$R_{ heta JC}$	4.8	°C/W

Static Electrical Characteristics (7)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250 \mu A$	25	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	0.4	-	1.2	V
	$V_{DS} = 25V, V_{GS} = 0V$ - $V_{DS} = 20V, V_{GS} = 0V,$ $T_{J} = 125^{\circ}C$ -	$V_{DS} = 25V, V_{GS} = 0V$	-	-	1	μА
Drain-to-Source Leakage Current		$V_{DS} = 20V, V_{GS} = 0V,$			10	
		-	10			
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0V, V_{GS} = \pm 10V$	-	-	±100	nA
Drain-to-Source On-Resistance	R _{DS(ON)}	$V_{GS} = 4.5V, I_D = 5A$	-	9.8	12	mΩ



Dynamic Electrical Characteristics (7)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Forward Transconductance	g _{fs}	$V_{DS} = 5V, I_{D} = 15A$	-	50	-	S
Total Gate Charge	Q_g	V _{GS} = 4.5V,	-	8.9	-	
Gate-to-Source Charge	Q_{gs}	V _{DS} = 15V,	-	3.7	-	nC
Gate-to-Drain Charge	Q_{gd}	I _D = 20A	-	2.2	-	
Turn-On Delay Time	t _{d(on)}	$V_{GS} = 10V, V_{DS} = 15V$ $I_{D} = 15A,$ $R_{G} = 3.0$	-	6	-	
Rise Time	t _r		-	3	-	
Turn-Off Delay Time	t _{d(off)}		-	18	-	ns
Fall Time	t _f		-	5	-	
Input Capacitance	C _{iss}	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1MHz	-	910	-	
Output Capacitance	C _{oss}		-	510	-	pF
Reverse Transfer Capacitance	C _{rss}		-	55	-	

Diode Characteristics (7)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Forward Voltage	V_{SD}	$V_{GS} = 0V$, $I_S = 10A$	-	0.9	-	V
Reverse Recovery Time	t _{rr}	$V_{GS} = 0V$, $I_S = 30A$,	-	17	-	ns
Reverse Recovery Charge	Q _{rr}	$dI_S/dt = 100A/\mu s$	-	8	-	μC

- (1) Rated according to $R_{\theta \text{JC}}.$
- (2) Rated according to $R_{\theta JA}. \label{eq:Relation}$
- (3) Limited by maximum T_J.
- (4) Starting T_J = 25°C, I_{AS} = 13A, L = 0.1mH, V_{DD} = 20V, V_{GS} = 10V
- (5) Pulse width limited by maximum $T_{\scriptscriptstyle J}$.
- (6) Surface-mounted on 1 inch² FR4 board, 2 oz Cu.
- (7) $T_J = 25$ °C unless otherwise specified.



Typical Electrical Characteristics

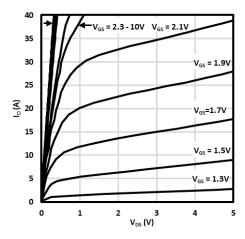


Fig.1 Output characteristics

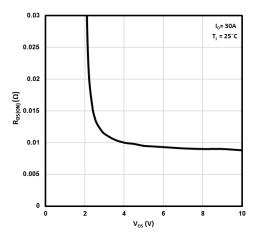


Fig.3 On-resistance vs. gate voltage

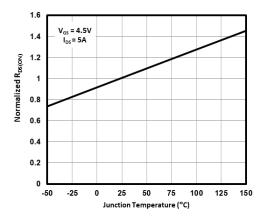


Fig.5 Normalized on-resistance vs. temperature

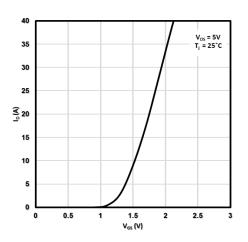


Fig.2 Transfer characteristics

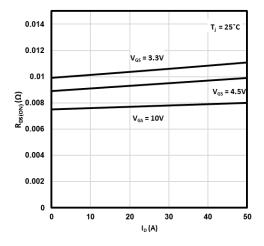


Fig.4 On-resistance vs. drain current

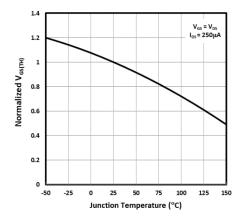


Fig.6 Normalized gate threshold voltage vs. temperature



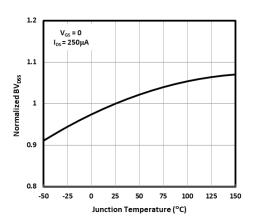


Fig.7 Normalized drain-to-source breakdown voltage vs. temperature

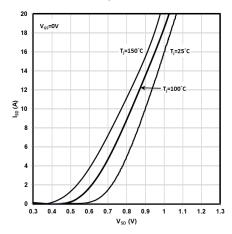


Fig.9 Source-to-drain diode forward characteristics

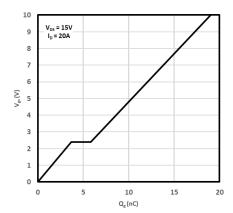


Fig.11 Gate-to-source voltage vs. gate charge

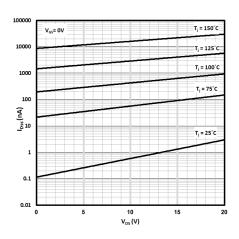


Fig.8 Drain-to-source leakage current vs. voltage

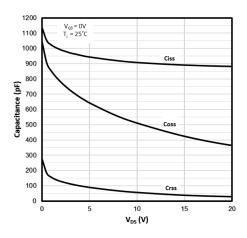


Fig.10 Capacitance vs. drain-to-source voltage

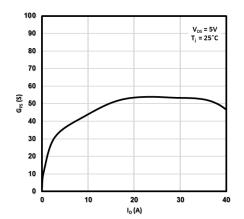


Fig.12 Transconductance



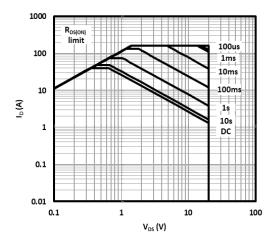


Fig. 13 Safe operating area

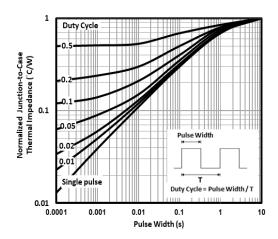


Fig. 14 Junction-to-ambient thermal impedance

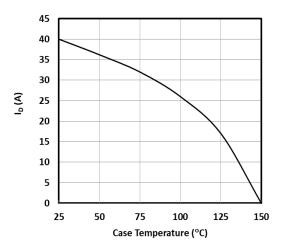


Fig.15 Maximum drain current vs. case temperature

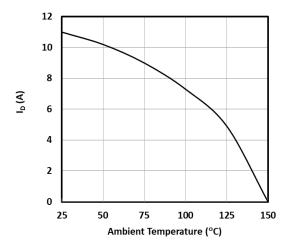
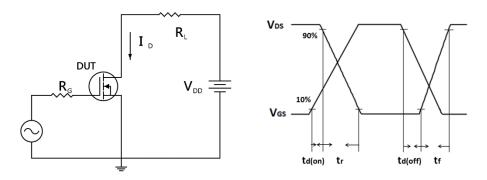


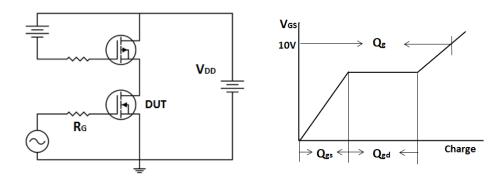
Fig.16 Maximum drain current vs. ambient temperature



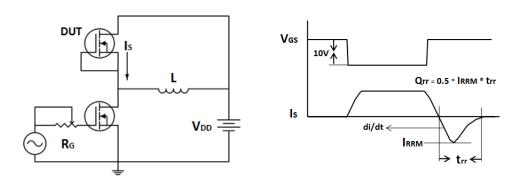
Test Circuits and Waveforms



Resistive switching time test circuit & waveforms

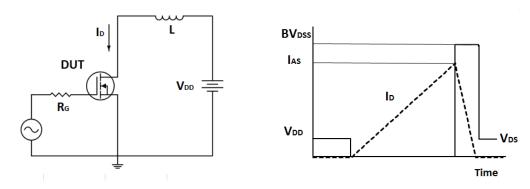


Gate charge test circuit & waveform



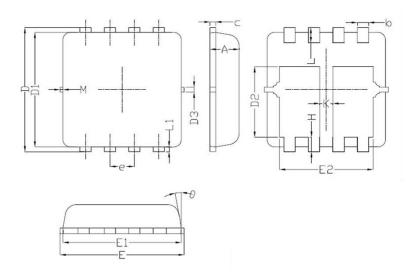
Peak diode recovery dv/dt test circuit & waveforms





Unclamped inductive switching test circuit & waveforms

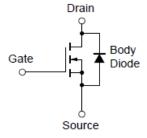
Package Drawing



SYMBOL	DIMENSONAL REQMTS			
STIVIBUL	MIN.	NOM.	MAX.	
Α	0.65	0.75	0.85	
b	0.20	0.30	0.40	
С	0.10	0.150	0.25	
D	3.15	3.35	3.45	
D1	3.00	3.10	3.20	
D2	1.54	1.88	1.94	
D3		0.13		
Ε	3.20	3.30	3.40	
E1	3.00	3.15	3.20	
E2	2.39	2.49	2.59	
е		0.65 BSC		
Н	0.30	0.39	0.50	
L	0.30	0.400	0.50	
LI		0.130		
K	0.30			
α		10°	12°	
М	*	*	0.15	
	* Not sp	ecified		

DFN 3.3x3.3

Equivalent Circuit







Revision history of JMT3801N Specification

Version	Change Items	Effective Date
1.00	Initial Release	09-Mar-20



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